Amendments to the Specification

On page 1, please amend the paragraph inserted between the title and the heading "BACKGROUND OF THE INVENTION" as follows:

--CROSS REFERENCE TO RELATED APPLICATIONS

This is a divisional application of application Serial No. 10/194,297, filed July 15, 2002, now U.S. Patent No. 6,720,794, which is hereby incorporated by reference in its entirety for all purposes.

Please replace the paragraph beginning on page 13, line 9 with the following amended paragraph:

For example, when the input signal IN rises from the "L" level (= VSS) to the "H" level (= VDD) at time t21, the output side nodes [[N121]] N12 and N13 of the inverters 12 and 13 fall down to the "L" level and the PMOS 18 becomes the ON state and the NMOS 19 becomes the OFF state. When the output side node N12 of the inverter 12 falls down to the "L" level, since the delay time DT of the delay circuit 24 is present, the output voltage of the delay circuit 24 is still at the "H" level and the NMOS 16 for pull up is in the ON state. Accordingly, the voltage divided by the inverter 12 and the NMOS 16 becomes voltage of the output side node N12 of the inverter 12. The PMOS 18 supplied with this divided voltage has a drive capacity made smaller and the voltage of the output signal OUT [[is]] slowly rises up to the "H" level via the PMOS 18.

Please replace the paragraph beginning on page 17, line 8 with the following amended paragraph:

Moreover, when the enable signal EN is at "L" level, the AND gate 34, the OR gate 35, the NAND gate 14A, and the NOR gate 15A are closed; output voltage of the AND gate 34 is fixed to "L" level; output voltage of the OR gate 35 is fixed to "H" level; output voltage of the NAND gate 14A is fixed to "H" level; and output voltage of the NOR gate 15A is fixed to "L" level. Accordingly, the output side node N12 of the inverter 12 is fixed to "H" level and the output side node N13 of the inverter 13 is fixed to "L" level. The "H" level output voltage of the NAND gate 14A makes the NMOS 16 in the ON state and the "L" level output voltage of the NOR gate 15A makes the PMOS 17 in the ON state. Accordingly, the node N12 is pulled up to the "H" level and the node N13 is pulled down to the "L" level. The PMOS 18 and NMOS 19 become the OFF state and the output terminal 20 becomes a Hiz state.

Please replace the paragraph beginning on page 20, line 8 with the following amended paragraph:

For example, it is assumed that the voltage fall of the diodes 42c and 42d is VTdio. In the inverter 120 of the present embodiment, the diodes [[diode]] 42c and 42d operate almost in the same way as the NMOS 12c and PMOS 12d in ~~Fig. 4~~ Fig. 2. Accordingly, when the input voltage is supplied to the input node Na, the output voltage of the output node Nb slowly changes in a voltage range between the ground potential

VSS and the voltage | VTdio | and a voltage range between the power source potential VDD and a voltage (VDD – | VTdio |). Consequently, the voltage of the output signal OUT of Fig. 1 also changes at a low speed.